

Fig. 1

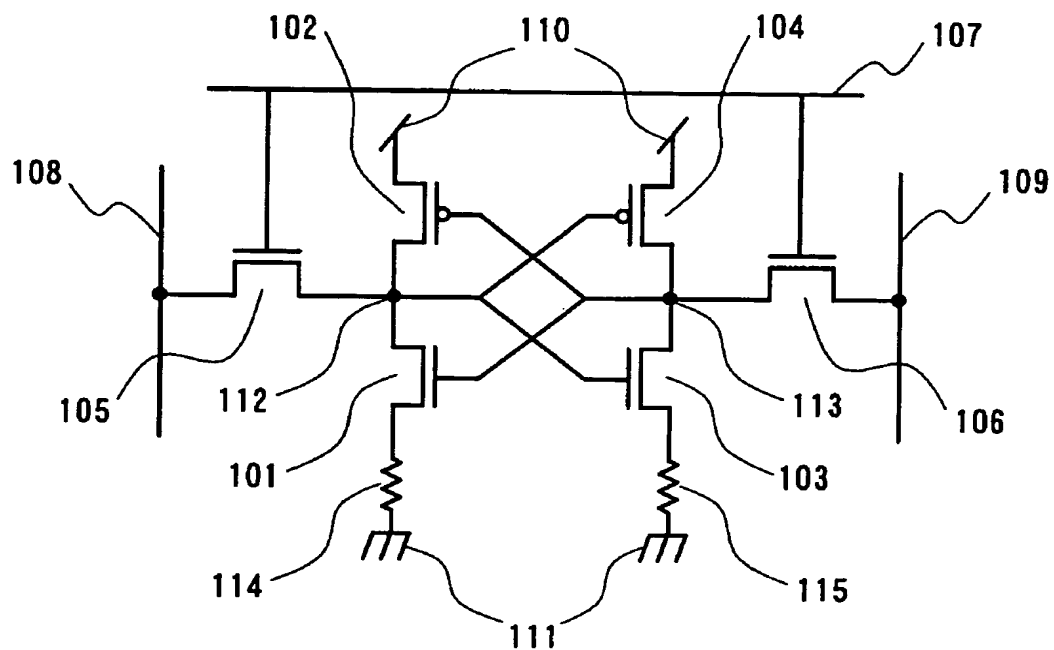


Fig. 2

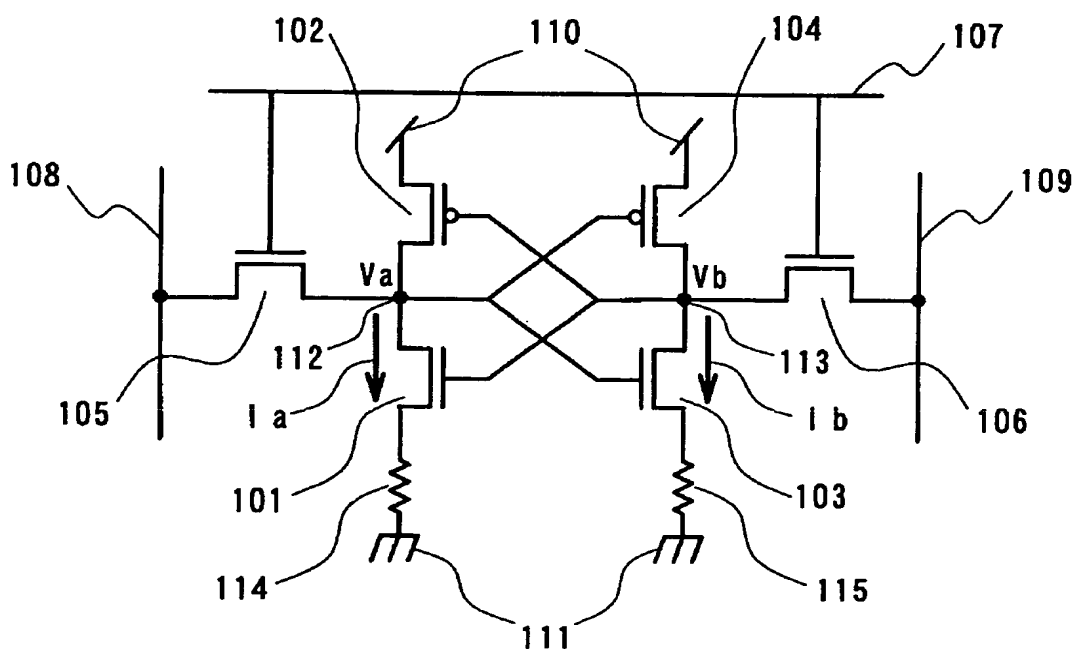
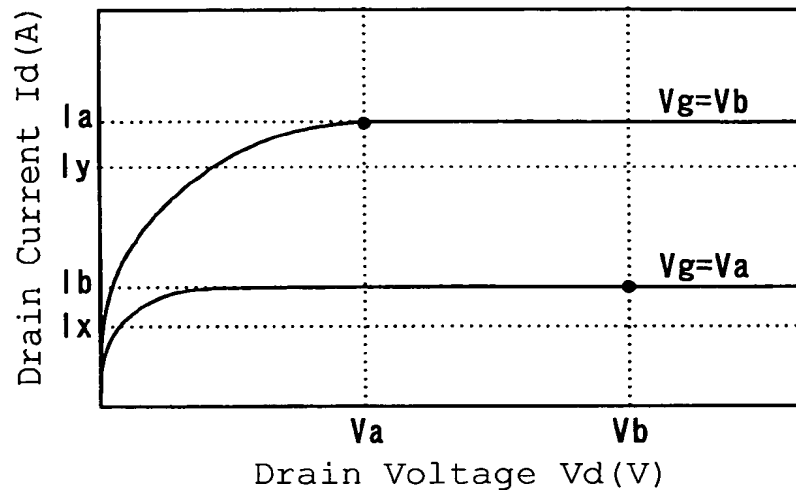


Fig. 3

(a)



(b)

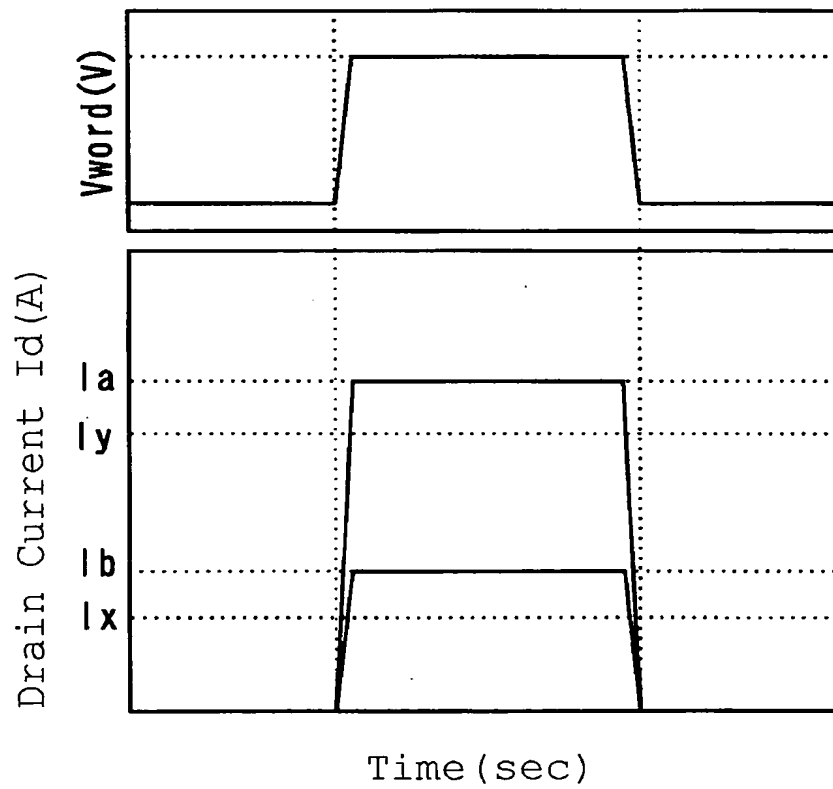


Fig. 4

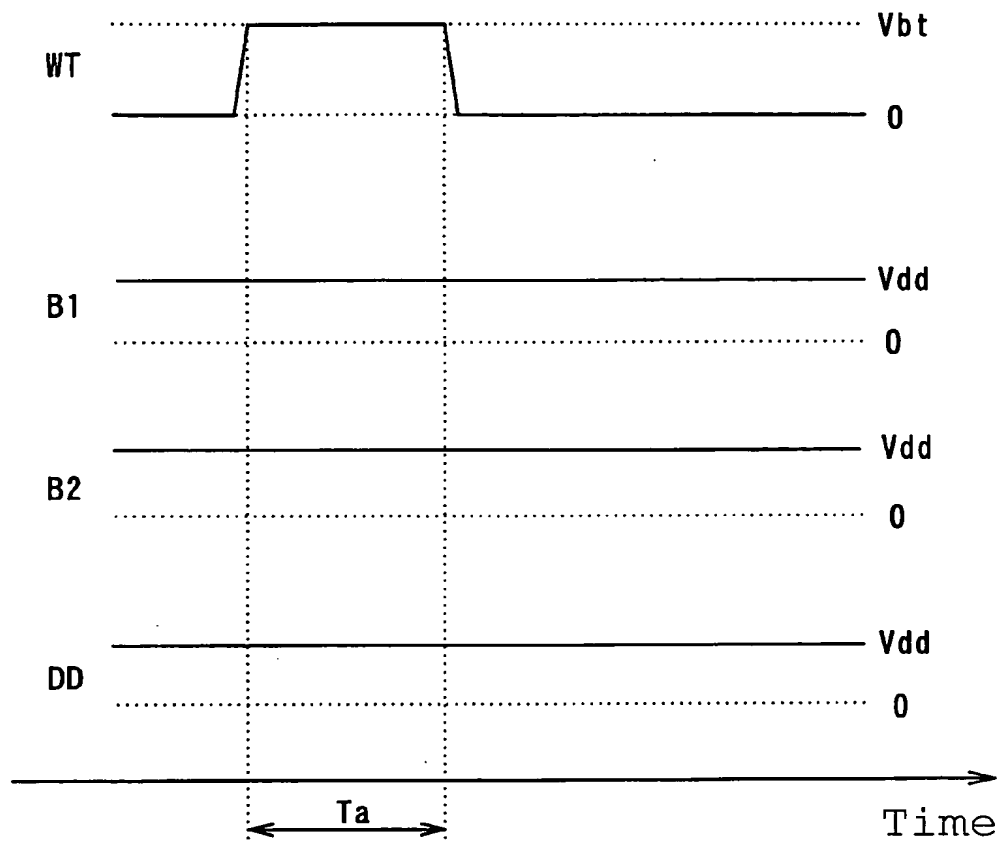


Fig. 5

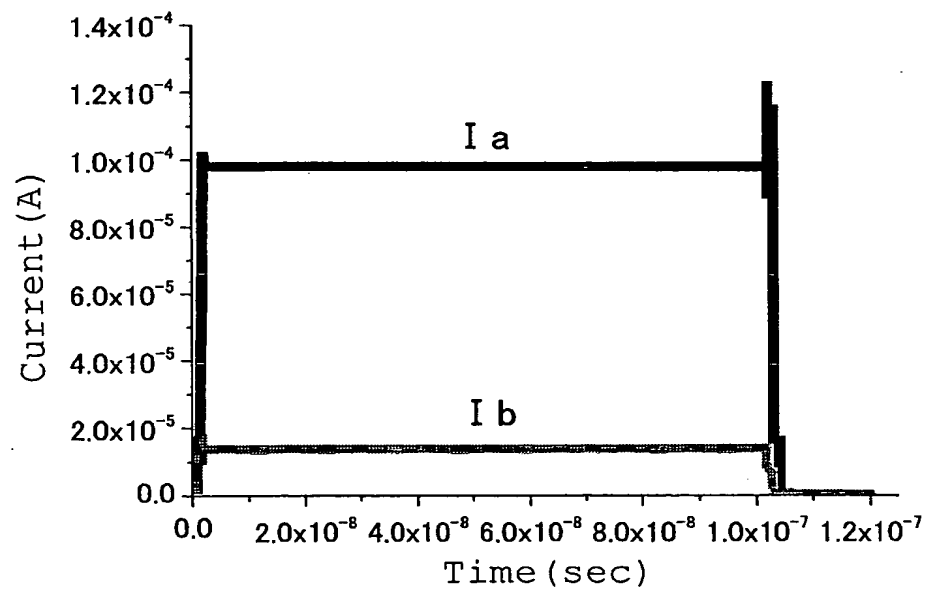


Fig. 6

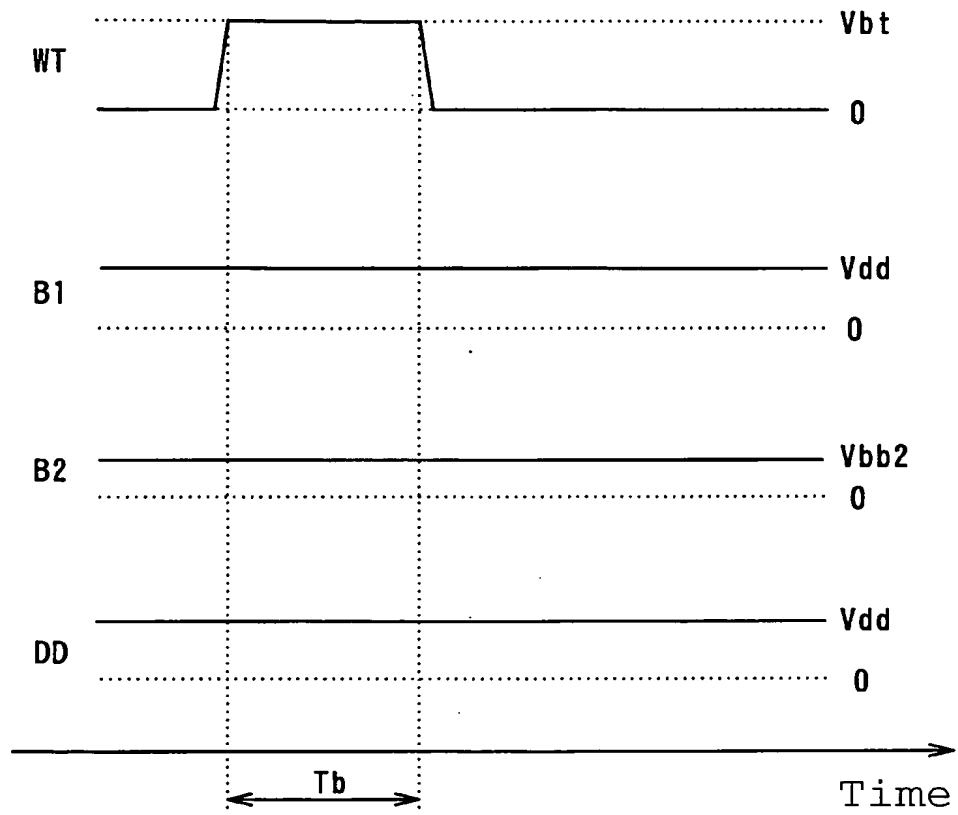


Fig. 7

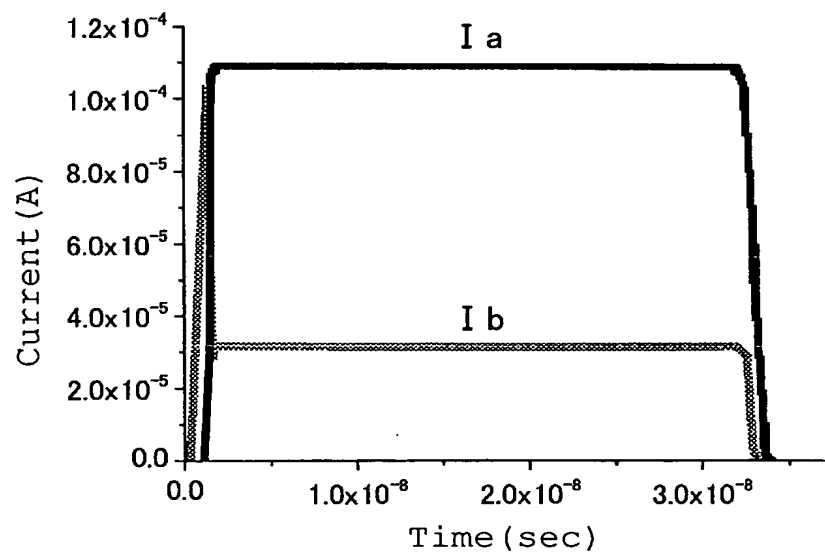


Fig. 8

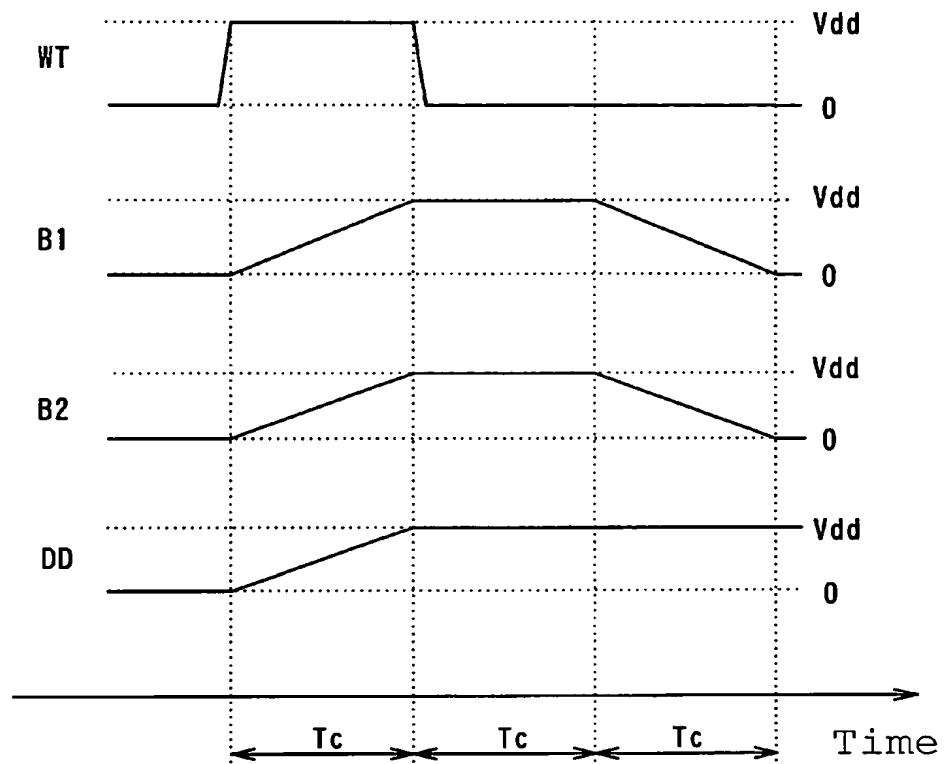


Fig. 9

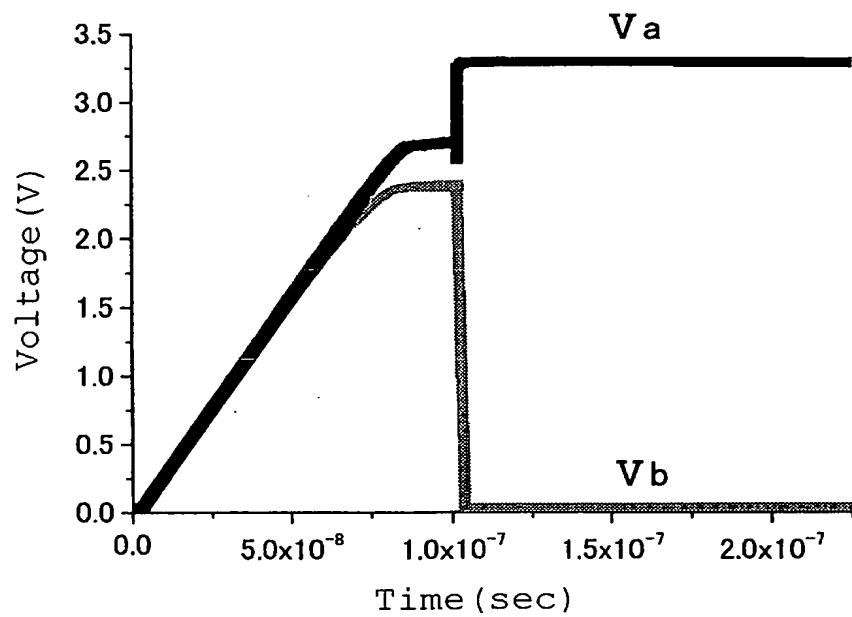


Fig. 10

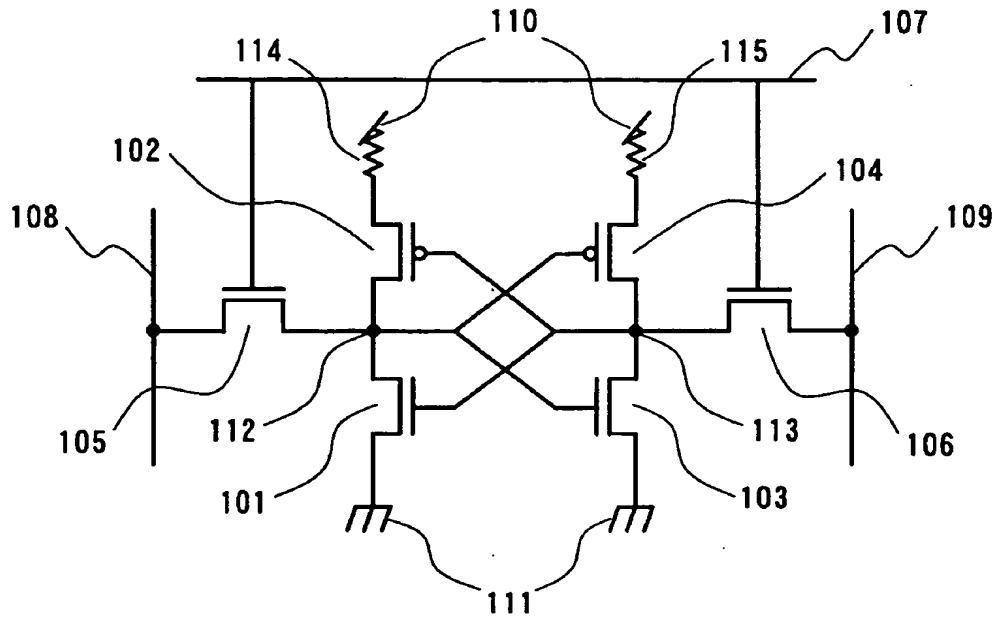


Fig. 11

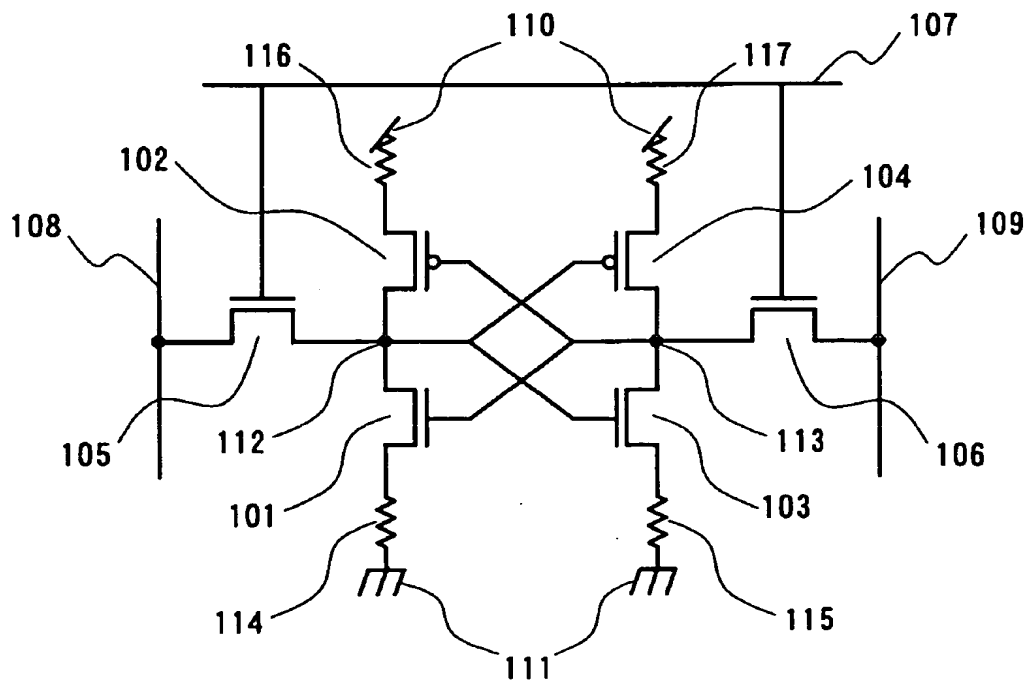
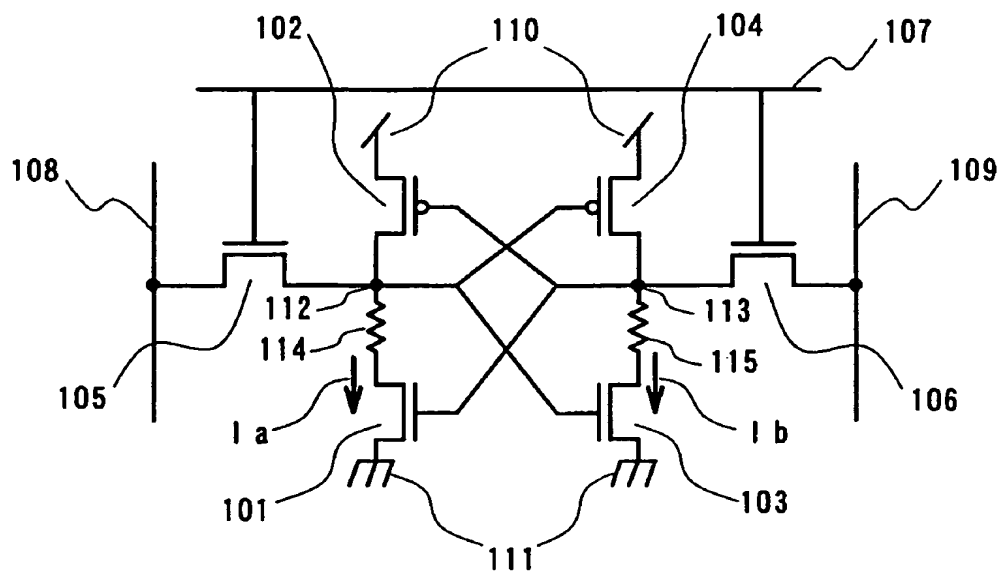
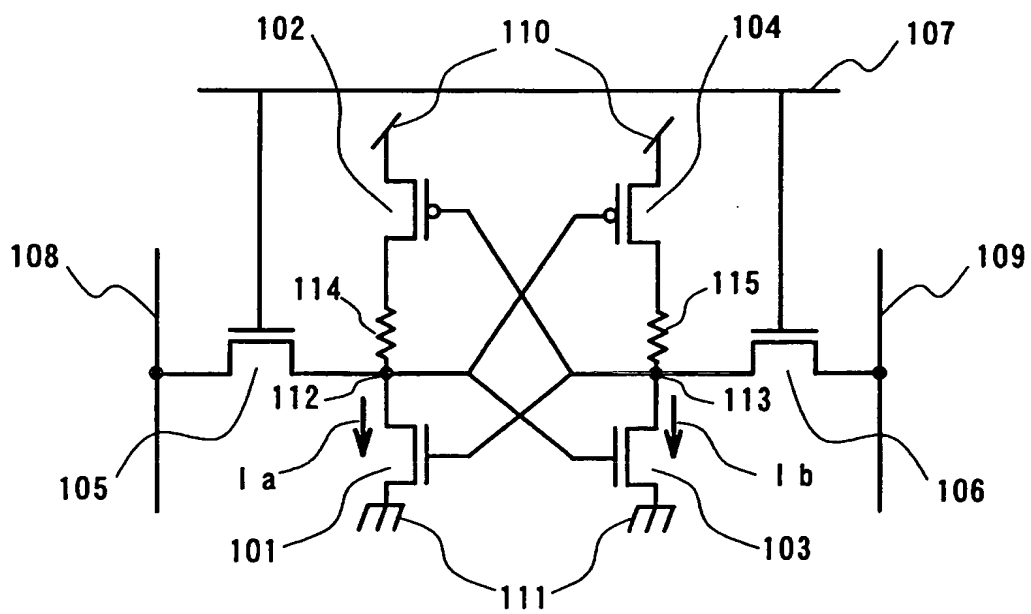


Fig. 12

(a)



(b)



(a)

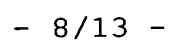
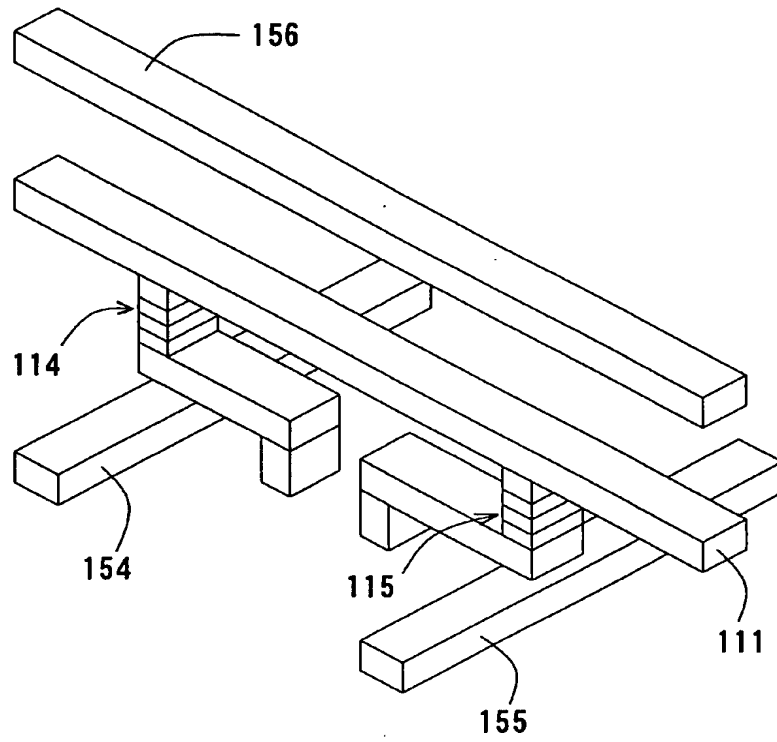


Fig. 14



[illegible]

The diagram shows a single unit cell of a crossbar array. It consists of a central diamond-shaped crossbar (110) connected to four access transistors (111, 112, 113, 114). The access transistors are connected to word lines (102, 104) and bit lines (105, 106). The central crossbar is connected to a data line (107). The access transistors are connected to a common source line (108) and a common drain line (109). The access transistors are labeled 101, 103, 105, and 107. The central crossbar is labeled 110. The word lines are labeled 102 and 104. The bit lines are labeled 105 and 106. The data line is labeled 107. The common source line is labeled 108. The common drain line is labeled 109.

Fig. 17

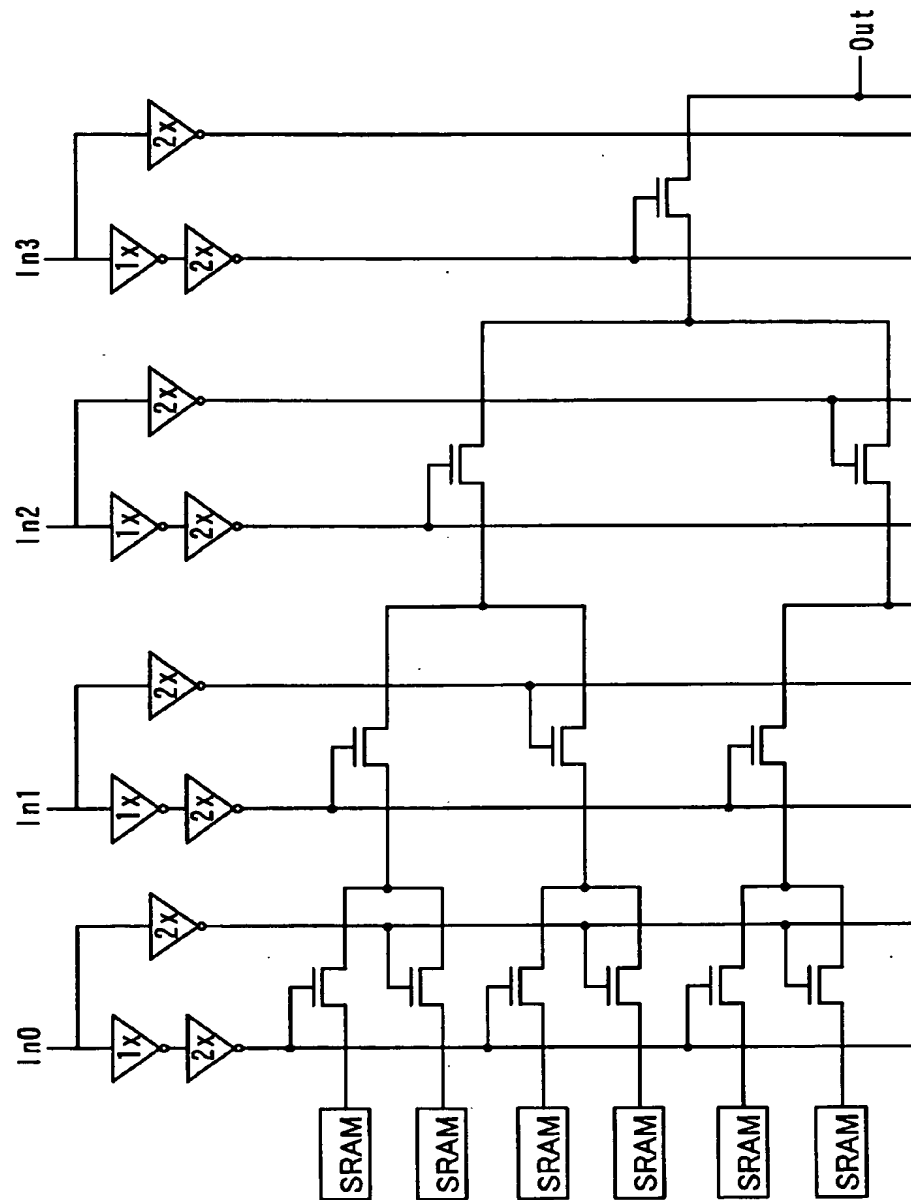


Fig. 18

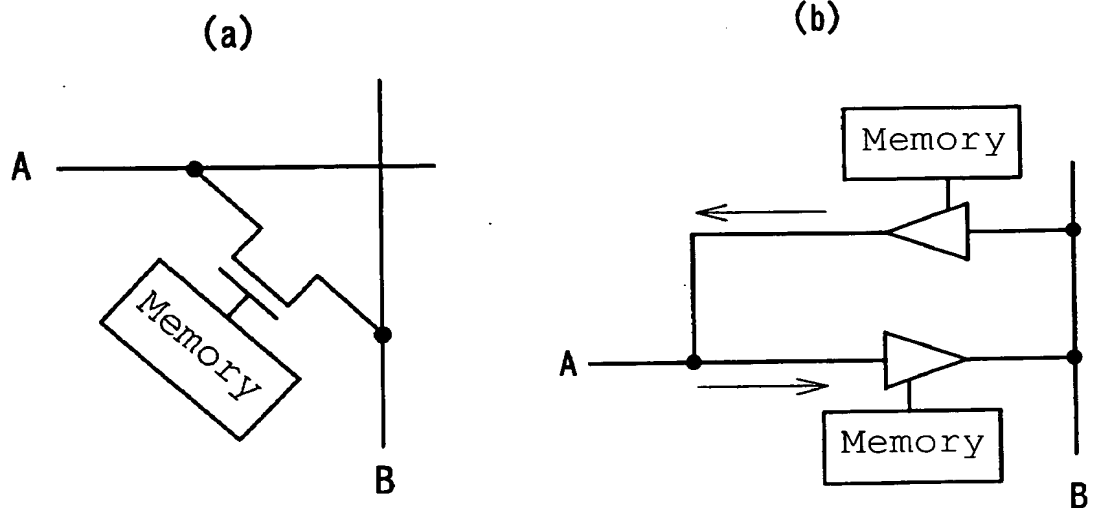


Fig. 19

PRIOR ART

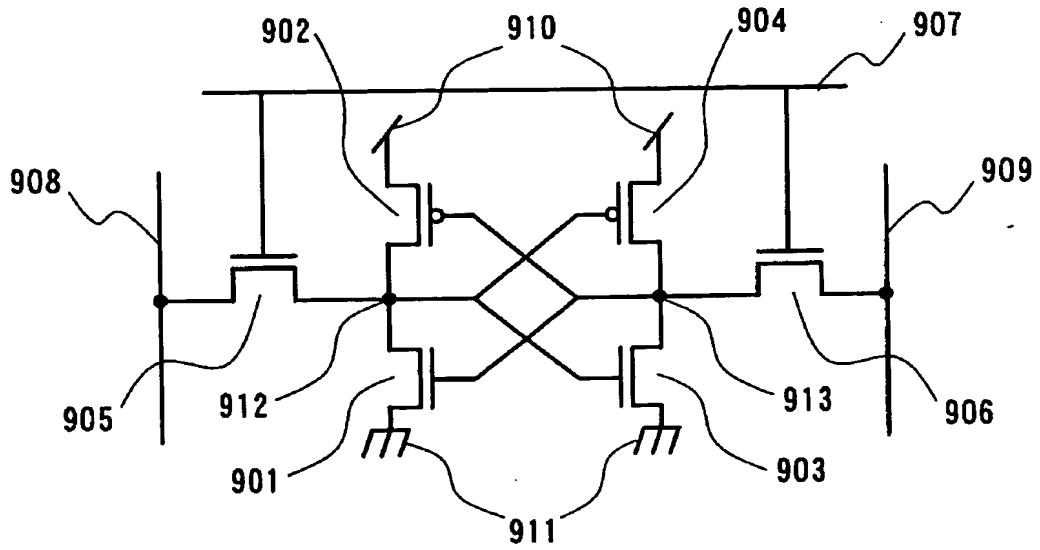


Fig. 20

PRIOR ART

